

REMARKS/ARGUMENTS

Claims 1, 2, 5-7, 11, 12, 15-19, and 21-25 are pending in the present application. Claims 5, 15, and 22 were amended in accordance with the Examiner's stated objection (Office Action dated September 17, 2007, page 3). Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 103, Obviousness

The Examiner rejects claims 1, 2, 5-7, 11, 12, 15-19 and 21-25 under 35 U.S.C. § 103 as obvious over Matsubara, et al., Information Processing System With Prefetch Instructions Having Indicator Bits Specifying Cache Levels for Prefetching, U.S. Patent No. 6,381,679, April 30, 2002, (hereinafter "Matsubara") in view of Anonymously Disclosed, Method for the Dynamic Prediction of NonSequential Memory Accesses, IP.com Electronic Publication, September 25, 2002, (hereinafter "Anonymous") and in further view of Ishimi, et al., Data Processor With Cache Memory, U.S. Patent No. 5,708,803, January 13, 1998, (hereinafter "Ishimi"). This rejection is respectfully traversed. In regards to claim 1, the Examiner states the following:

As per claims 1 and 18, Matsubara discloses a method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction (col. 5, lines 1-10; col. 6, lines 35-42 and 53-55; col. 7, lines 10-20; Fig. 1; Fig. 2, elements 21 and 22; Fig. 68). *It should be noted that computer program product in claims 18-19 and 21-24 executes the exact same functions as the methods in claims 1-2 and 4-7. Therefore, any references that teach claims 1-2 and 4-7 also teach the corresponding: claims 18-19 and 21-24. It should also be noted that the "indication bits (i.e. PF bits)" equaling 1 is analogous to the "prefetch indicator being associated with the instruction" and the "CPU 21" is analogous to the "processor unit." Lastly, it should be noted that the "instruction fetch (IF)" stage is when the instruction in the code is loaded into a cache and the "decoding" stage is when the "determination" is made.*

and responsive to the prefetch indicator being associated with the instruction, selectively prefetching data into the cache in the processor (col. 6, lines 53-55; Fig. 2, elements 21 and 22). *It should be noted that when it is determined that the value of the PF bits is 1, all the data of the line is prefetched to the primary cache.*

Matsubara does not expressly disclose a pointer to a data structure identified by the prefetch indicator; wherein the selectively prefetching step includes:

determining whether outstanding cache misses are present; and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.

Anon discloses a pointer to a data structure identified by the prefetch indicator (General Description, 1st paragraph and 4th paragraph; Detailed Description, 1st paragraph). *It should be noted that the "dynamic prefetch pointer" is analogous to the "pointer to a data structure."*

Matsubara and Anon are analogous art because they are from the same field of endeavor, that being prefetching memory systems. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Anon's dynamic prefetch pointer within Matsubara's information processing system. The motivation for doing so would have been to improve memory access due to improved memory access prediction and also improve performance due to reducing the time spent waiting for memory accesses to complete (Anon, General Description, 5th paragraph).

The combination of Matsubara/Anon does not expressly disclose wherein the selectively prefetching step includes:

- determining whether outstanding cache misses are present; and
- prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.

Ishimi discloses wherein the selectively prefetching step includes: determining whether outstanding cache misses are present (col. 13, line 30; Fig. 13, element 84) and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold (col. 13, lines 30-32; Fig. 13, element 810). *It should be noted that the threshold is equal to 1. Thus, when it is determined there is a cache hit, meaning there are zero outstanding cache misses (i.e. the number of outstanding cache misses is than the threshold of 1), data is prefetched.*

The combination of Matsubara/Anon and Ishimi are analogous art because they are from the same field of endeavor, that being prefetching memory systems. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Ishimi's fetch mechanism within Matsubara/Anon's information processing system. The motivation for doing so would have been to provide a data processor capable of processing quickly by lessening the number of abortions even when a branch prediction is preformed (Ishimi, col. 3, lines 3-6). Therefore, it would have been obvious to combine Matsubara, Anon, and Ishimi for the benefit of obtaining the invention as specified in claims 1 and 18.

Office Action dated August 24, 2007, pages 3-6.

The Examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. §103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). Additionally, all limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Therefore, no *prima facie* obviousness rejection can be established if the proposed combination does not teach all of the features of the claimed invention. Furthermore, if an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

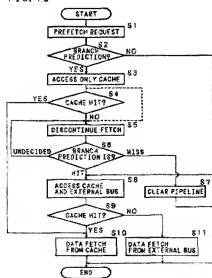
Claim 1 is as follows:

1. A method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:
 - responsive to loading an instruction in the code into a cache,
 - determining, by a processor unit, whether a prefetch indicator is associated with the instruction; and
 - responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor, wherein the selectively prefetching step includes:
 - determining whether outstanding cache misses are present; and
 - prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.

The Examiner fails to present a *prima facie* case of obviousness because the combination of references, considered as a whole, fails to teach or suggest all of the features of claim 1. For example, the proposed combination of references, considered as a whole, does not teach or suggest the features of, “determining whether outstanding cache misses are present; and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.” as recited in claim 1.

The Examiner admits, as cited above, that the combination of *Matsubara* and *Anonymous* does not teach the above recited features of claim 1. However, the Examiner asserts that *Ishimi* teaches the features of, “determining whether outstanding cache misses are present; and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold,” as recited in claim 1. The Examiner cites to the following portion of *Ishimi*:

FIG. 13



As a result, when the cache hit occurs (step S4), data is fetched from the cache memory in the operand access unit 1 (step S10).

Ishimi, Figure 13, and col. 13, lines 30-32.

Ishimi does not teach or suggest the features of, “determining whether outstanding cache misses are present; and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold,” as recited in claim 1. In order to make a determination that a number of outstanding cache misses is less than a threshold, a determination must be made between a number of outstanding cache misses value and a threshold value. *Ishimi* is devoid of any teaching in regards to making a determination between a number of outstanding cache misses value and a threshold value.

As depicted in *Ishimi*’s Figure 13, cited above, at S9, a determination is made as to whether there is a cache hit or a cache miss. If there is a cache hit, meaning the requested data is presently stored in the cache, the data is fetched from the cache (*Ishimi*, Figure 13, S10). If there is a cache miss, meaning the requested data is not presently stored in the cache, the data is fetched from the external bus (*Ishimi*, Figure 13, S11). In either scenario, the data is fetched. *Ishimi* does not teach the feature of making a determination that a number of outstanding cache misses is less than a threshold.

The Examiner states, “It should be noted that the threshold is equal to 1,” (Office Action dated August 24, 2007, page 5). However, *Ishimi* provides no support for such a statement. *Ishimi* is devoid of any teachings in regards to maintaining threshold value. In addition, *Ishimi* is devoid of any teachings in regards to determining the number of outstanding cache misses. *Ishimi* simply determines if there is a cache hit or miss (*Ishimi*, Figure 13, S9) and fetches the data from the appropriate location (*Ishimi*, Figure 13, S10 and S11). Accordingly, *Ishimi* does not teach prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold,” as recited in claim 1.

Because the Examiner admits that the combination of *Matsubara* and *Anonymous* does not teach the features of, “determining whether outstanding cache misses are present; and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold,” as recited in claim 1 and because *Ishimi* does not teach the above recited features of claim 1, the combination of references, considered as a whole, fails to teach or suggest all of the features of claim 1. Accordingly, the Examiner fails to present a *prima facie* case of obviousness in regards to claim 1.

Furthermore, rejections based on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *Teleflex Inc. v. KSR Int’l Co.*, 550 U.S. at 1, 82 USPQ2d at 1396 (2007). In the case at hand, the Examiner fails to state a *prima facie* case of obviousness because the Examiner failed to provide articulated reasons, with some rational underpinning to support the legal conclusion of obviousness, as to why one of ordinary skill in the art would be led to combine the teachings of the references.

In combining the references the Examiner states, “The motivation would have been to provide a data processor capable of processing quickly by lessening the number of abortions even when a branch

prediction is performed (*Ishimi*, col. 3, lines 3-6)," (Office Action dated September 17, 2007, page 6). However, based on the Examiner's statement, *Ishimi* already provides a data processor capable of processing quickly by lessening the number of abortions even when a branch prediction is performed. Accordingly, no need, reason, or motivation exists for combining the teachings of two additional references. Therefore, the Examiner has not satisfied the requirement of articulating a reason with some rational underpinning to support the legal conclusion of obviousness as required under *KSR* as to why one of ordinary skill in the art would look to combine the teachings of the references. Consequently, the Examiner's obviousness rejection cannot be sustained.

Because the remaining claims either depend from or recite similar features as those recited in claim 1, the same distinctions vis-à-vis claim 1 and *Ishimi* apply to the remaining claims. Furthermore, various dependent claims recite additional features which are not disclosed or suggested by the cited art. For example, claim 4, which depends from claim 1, recites, in part, "prefetching the data in response to a determination that a number of cache lines chosen to be replaced is greater than a threshold." As discussed above, the cited art, including *Ishimi*, is devoid of any teachings in regards to maintaining threshold values. Claim 4, accordingly, and corresponding claims 14 and 21 patentably distinguish over the cited art in their own right as well as by virtue of their dependency.

Therefore, the rejection of claims 1-2, 5-7, 11-12, 15-19 and 22-24 under 35 U.S.C. § 103 has been overcome.

II. Conclusion

The subject application is patentable over the cited references and should now be in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: December 20, 2007

Respectfully submitted,

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